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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,506	12/09/1999	TAE-GYOUNG KANG	5484-53	8916

7590 05/28/2004

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AM

Office Action Summary	Application No.	Applicant(s)	
	09/458,506	KANG, TAE-GYOUNG	
	Examin r	Art Unit	
	ori nadav	2811	

-- Th MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-25,29-38,40-46 and 48-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-25,33-35,40-45,52 and 53* is/are allowed.

6)☒ Claim(s) *29-32,36-38,46,48-51 and 54-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 54-59 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support for the dummy gates being formed on an isolation portion which belong (of) to an active region of transistor gates, as recited in claim 54.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 54-59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of an isolation portion of said active region and first dummy gates on said isolation portion, as recited in claim 54, are unclear as to how an isolation portion belong (of) to an active region and how dummy

gates can be formed on an isolation portion which belong to an active region of transistor gates.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 29, 36-37, 46 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Bothra et al. (6,020,616).

Regarding claims 29 and 36-37, Bothra et al. teach in figure 3L and related text a semiconductor device comprising a substrate with a plurality of active regions 204 and a plurality of inactive regions 214, each active region having at least one source region and at least one drain region;

a plurality of transistor gates 216, each transistor gate having at least one gate extension that extends over one of the plurality of active regions between the at least one source region and the at least one drain region; and

a plurality of dummy gates 226 (column 5, lines 35-60), each dummy gate having at least one dummy gate

extension that extends over one of the plurality of inactive regions, where each of the dummy gate extensions and each of the gate extensions are elements of a group, where each element of the group is parallel to at least two other elements of the group and all elements of the group are uniformly spaced across a width of the substrate, wherein a length of the gate extensions and the dummy gate extensions is variable.

Regarding the claimed limitation of gate extension, Bothra et al. teach a gate extension, because the gate extension is an integral part of the gate, and thus being indistinguishable from the gate.

Regarding the claimed limitations of "each element of the group is parallel to at least two other elements of the group and all elements of the group are uniformly spaced across a width of the substrate", note that an element of the group can be any entity, and does not necessarily has to be a dummy gate extension or a gate extension.

Regarding claim 46, Bothra et al. teach in figure 4A and related text each dummy gate being in contact with a bias line.

Regarding claim 50, Bothra et al. teach in figure 3L a plurality of dummy gates 226 commonly connected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

1. Claims 30-32 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra et al. (6,020,616) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 30 and 31, Bothra et al. teach substantially the entire claimed structure, as applied to claim 29 and 54 above, except a first metal being connected to the at least one source region and the at least one drain region by a plurality of contacts and a second metal is connected to a first part of the first metal to supply a voltage. AAPA teaches in figure 5 and related text a first metal ME2 (figure 9) connected to the source and drain regions by a plurality of contacts 70, and a second metal 64 connected to a first part of the first metal to supply voltage.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to a first metal being connected to the at least one source region

and the at least one drain region by a plurality of contacts and a second metal being connected to a first part of the first metal to supply a voltage in Bothra et al., in order to be able to operate the device.

Regarding claim 32, Bothra et al. teach in figure 3L a plurality of dummy gates 226 commonly connected to a ground voltage (column 5, lines 40-50). AAPA teaches in figure 10 a second metal ME3 connected to a second part of the first metal to supply ground voltage (page 7, lines 17-21). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the plurality of dummy gates commonly connected to a second part of the first metal to supply ground voltage, in Bothra et al.'s device in order to suppress the inductive noise of the device. The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates commonly connected to a ground voltage (column 5, lines 40-50),

Regarding claim 49, APA teaches in figure 5 at least two transistor gates P2G, P3G have a common terminal. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form at least two transistor gates with a common terminal in Bothra et al.'s device I order to use the device I an application which requires such configuration.

Claims 48 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra et al. in view of Hansch et al. (6,174,741).

Regarding claims 48 and 51, Bothra et al. teach substantially the entire claimed structure, as applied to claim 46 above, except stating that the length and the width of the dummy gates are substantially the same as those of the transistor gates.

Hansch et al. teach in figures 3B and 4 the length and width of dummy gates DG, DGL are substantially the same as those of the transistor gates G, GL, respectively.

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the length and width of the dummy gates substantially the same as those of the transistor gates, as taught by Hansch et al., in the device of Bothra et al. in order to simplify the processing steps of making the device by forming the transistor gates and the dummy gates with the same width and length..

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra et al. in view of Neugebauer (5,748,835).

Regarding claim 38, Bothra et al. teach substantially the entire claimed structure, as applied to claims 36 and 37 above, except a second dimension being a transistor gate width, i.e. a plurality of transistor gates having substantially identical length and width dimensions.

Neugebauer teaches a plurality of transistor gates having substantially identical length and width dimensions (column 13, lines 6-8).

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of transistor gates having substantially identical length and width dimensions as taught by Neugebauer, in the device of Bothra et al., in order to minimize the error of each of the channel coupled semiconductors when using the device in channel coupled feedback circuits.

Claims 54-56 and 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Nagamine (5,534,724) and Bothra et al. (6,020,616).

Regarding claim 54, AAPA teaches in figure 5 and related text pages (1-3 and 5-7) a semiconductor device comprising: a substrate; a rectangular region on the substrate; an active region having a first width and a second width on said rectangular region; an isolation portion of said active region on said rectangular region; first transistor gates on said first width of said active region; second transistor gates on said second width; wherein said first width is less than said second width;

and

AAPA does not teach dummy gates such that: first dummy gates on said isolation portion aligned with said first transistor gates such that a portion of a first dummy gate extending in a first direction and a portion of a corresponding first transistor gate extending in the first direction share a common central axis, and wherein said transistor gates and said first dummy gates are of substantially identical gap between gates.

Nagamine teaches in figure 3 and related text a semiconductor device comprising a substrate (column 5, line 10) and a plurality of dummy gates 20 having a predetermined width and length (figure 1), such that the transistor gates and said first dummy gates are of substantially identical gap between gates (figure 4 and column 6, lines 19-24).

Bothra et al. teach in figure 3L and related text a first dummy gates on said isolation portion (figure 2) aligned with said first transistor gates such that a portion of a first dummy gate extending in a first direction and a portion of a corresponding first transistor gate extending in the first direction share a common central axis, and wherein said transistor gates and said first dummy gates are of substantially identical gap between gates.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form AAPA's device on a substrate wherein first dummy gates on said isolation portion aligned with said first transistor gates such that a portion of a first dummy gate extending in a first direction and a portion of a corresponding first transistor gate extending in the first direction share a common central axis, and wherein said transistor gates and said first dummy gates are of substantially identical gap between gates, in order to support the device (by providing a substrate there under), to reduce the inductive noise of the device (by providing a plurality of dummy gates having a predetermined width and length between outside ones of the transistors) and in order to simplify the processing steps of making the device (by providing a substantially identical gap there between and an identical gap between the dummy gates and adjacent transistor gate), respectively.

The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates having a predetermined width and length between and outside adjacent transistors (figure 3L and column 2, lines 61-67), and by the teachings of Nagamine who points out the advantages of forming a plurality of dummy gates at a substantially identical gap there between as that between the adjacent ones of the transistor gates (column 2, lines 38-41),

Regarding claims 55-56 and 58-59, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Nagamine and Bothra et al., as applied to claim 54 above, and further in view of Hansch et al. (6,174,741).

Regarding claim 57, AAPA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as applied to claim 54 above, except stating that the length and the width of the dummy gates are substantially the same as those of the transistor gates. Hansch et al. teach in figures 3B and 4 the length and width of dummy gates DG, DGL are substantially the same as those of the transistor gates G, GL, respectively.

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the length and width of the dummy gates substantially the same as those of the transistor gates, as taught by Hansch et al., in the device of AAPA, Nagamine and Bothra et al. in order to simplify the processing steps of making

the device by forming the transistor gates and the dummy gates with the same width and length..

Response to Arguments

Applicant's arguments with respect to claims 29-32, 36-38, 46, 48-51 and 54-59 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 14-25, 33-36, 40-45 and 52-53 are allowed.

Reasons for allowance

The following is an examiner's statement of reasons for allowance:

Regarding claims 14, 18 and 22, Admitted Prior Art (APA), Nagamine (5,534,724) and Bothra et al. (6,020,616) appear to be the closest prior art reference. APA, Nagamine and Bothra et al. teach substantially the entire claimed structure as recited in claims 14, 18 and 22, except a plurality of dummy gates having the predetermined width and length located between two transistors, as recited in claims 14 and 18, and located not between but to both sides of the two transistors, as recited in claim 22.

Regarding claim 33, Admitted Prior Art (APA), Nagamine (5,534,724) and Bothra et al. (6,020,616) appear to be the closest prior art reference. APA, Nagamine and Bothra et al. teach substantially the entire claimed structure as recited in claim 33, except third

and fourth gaps between first and second transistor gates (at an edge of the first and second active regions) and first and second dummy gates (at an edge of the first and second portions) are substantially identical to each other and to first and second gaps. Regarding claims 52 and 53, Admitted Prior Art (APA), Nagamine (5,534,724) and Bothra et al. (6,020,616) appear to be the closest prior art reference. APA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as recited in claims 52 and 53, except a plurality of dummy gates having a portion extending in a first direction and a plurality of portions extending in a second direction perpendicular to the first direction. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). Th Group 2811 Fax Center number is (703) 308-7722

and 308-7724. The Group 2811 Fax Center is to be us d only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
5/25/04

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800